

1 / 1 4

FIG. 1

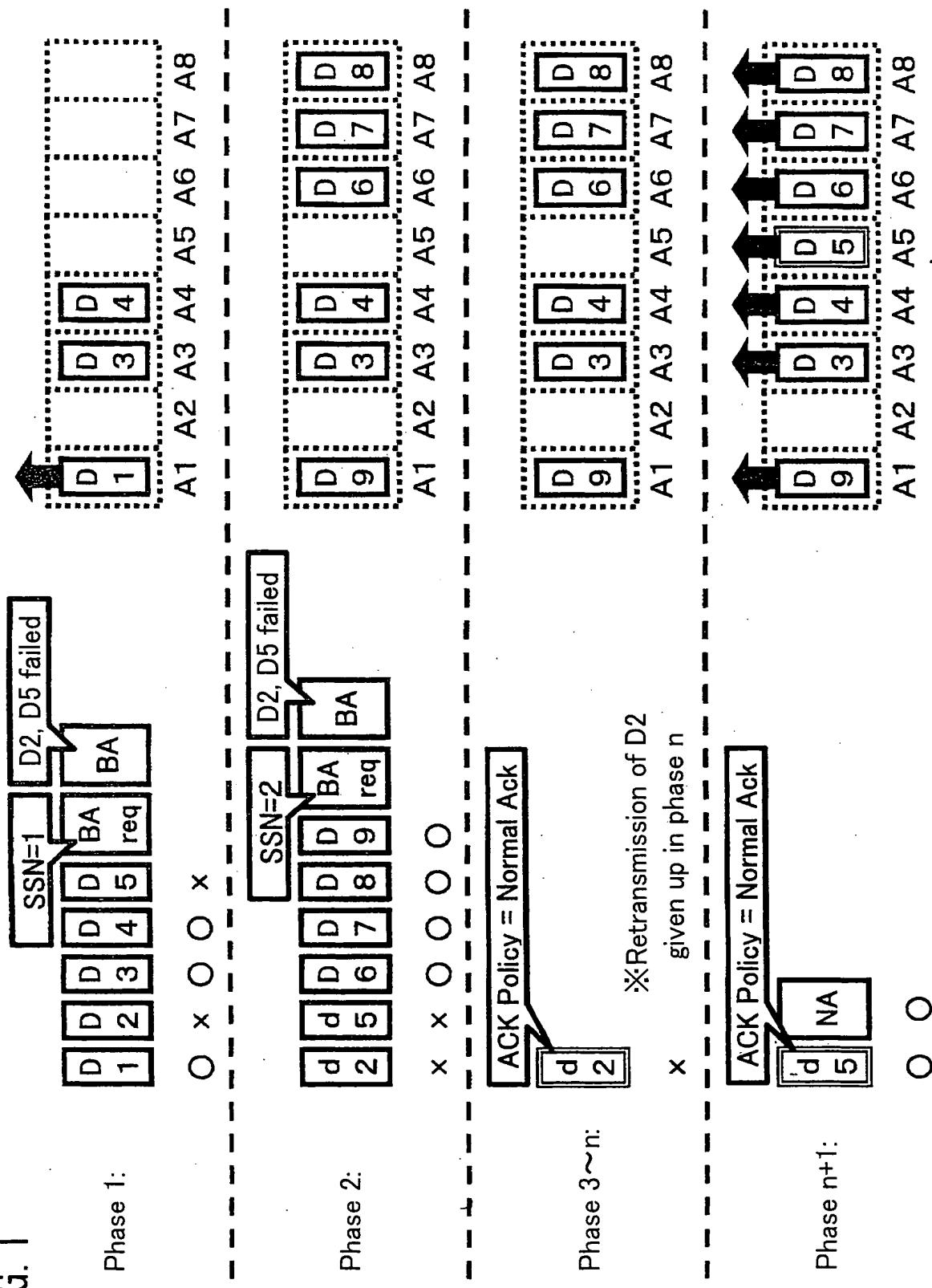
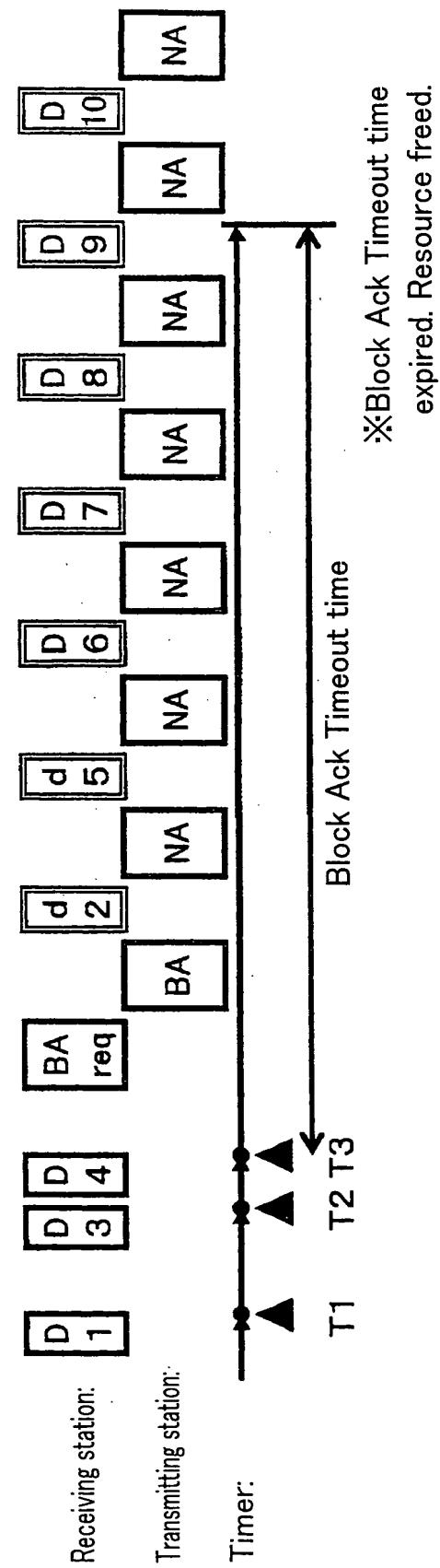
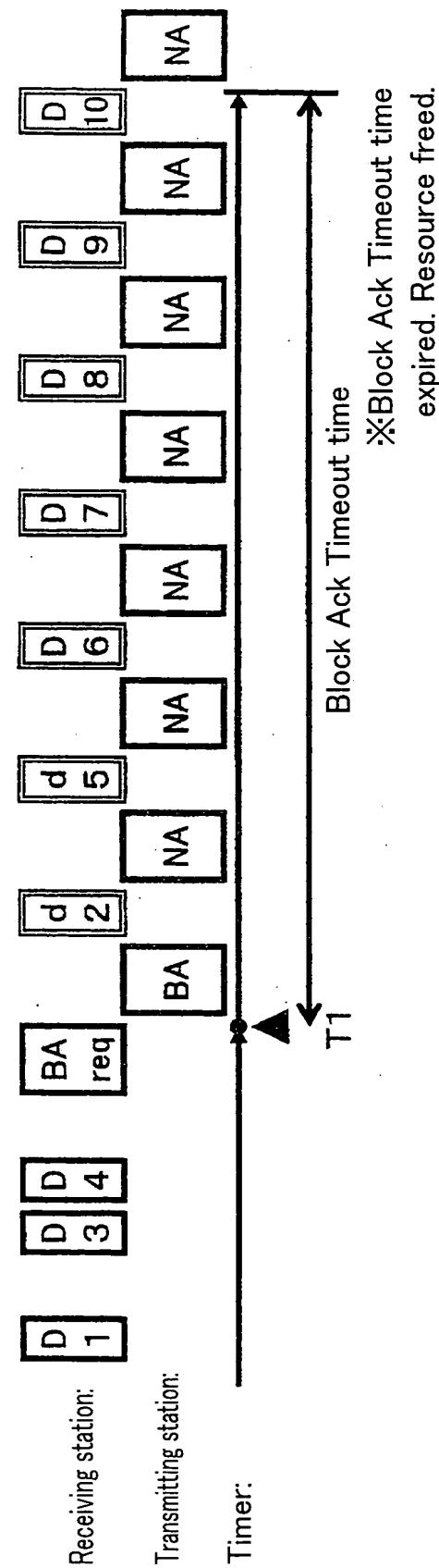


FIG. 2



3 / 1 4

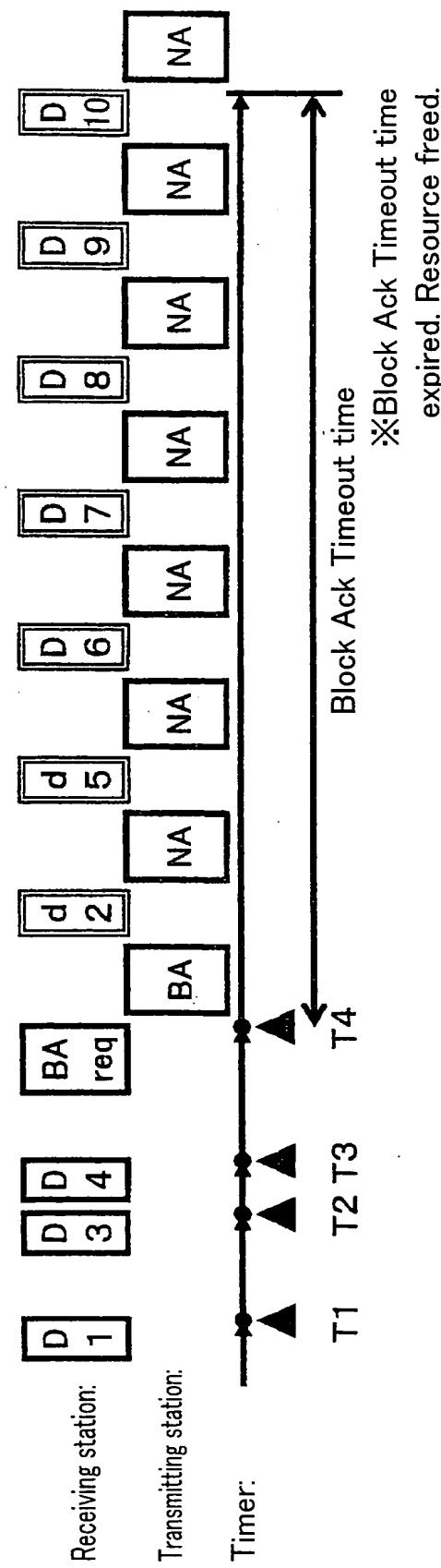
FIG. 3



▲ : Timer reset

4 / 1 4

FIG. 4



▲ : Timer reset

5 / 1 4

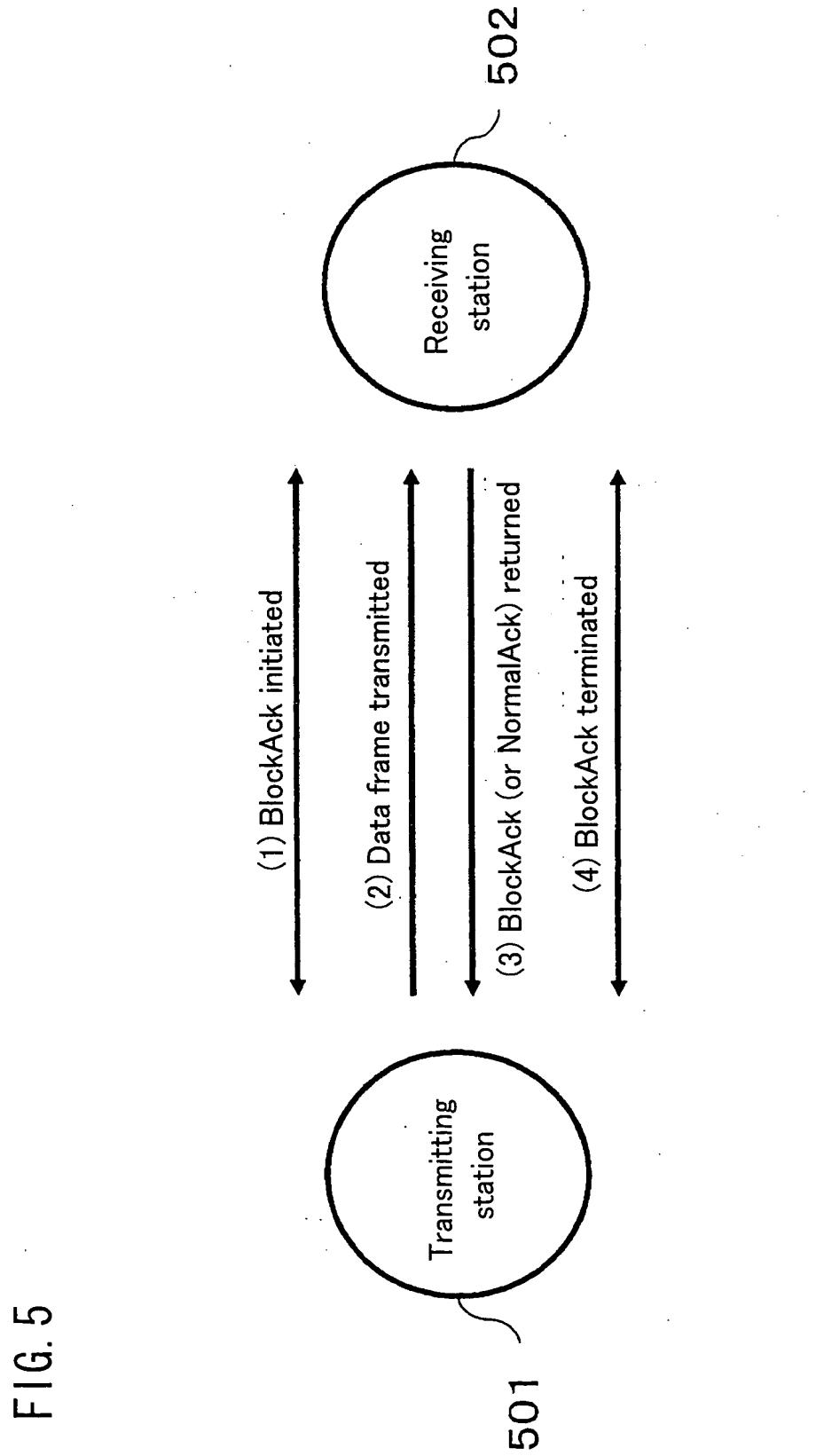
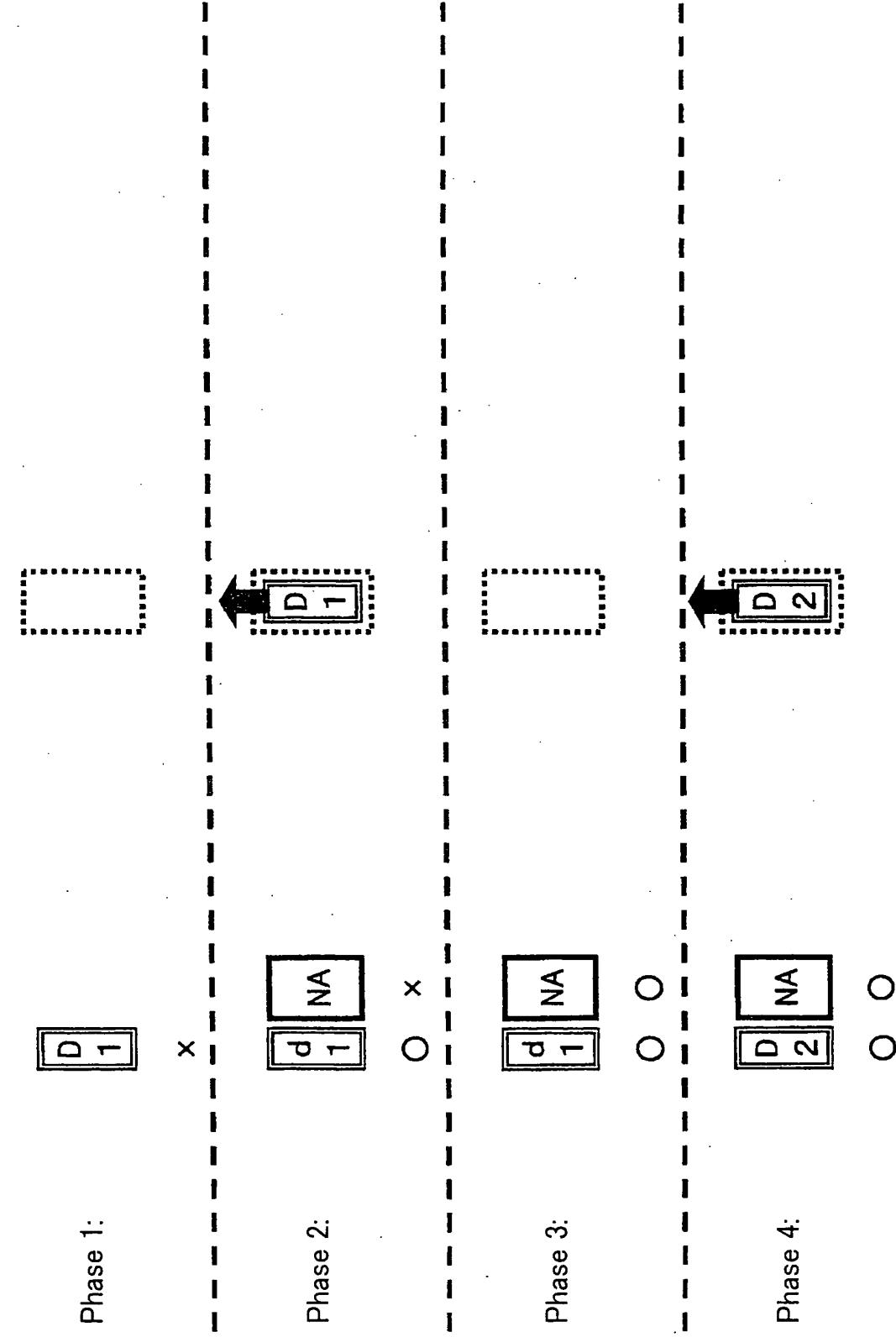


FIG. 5

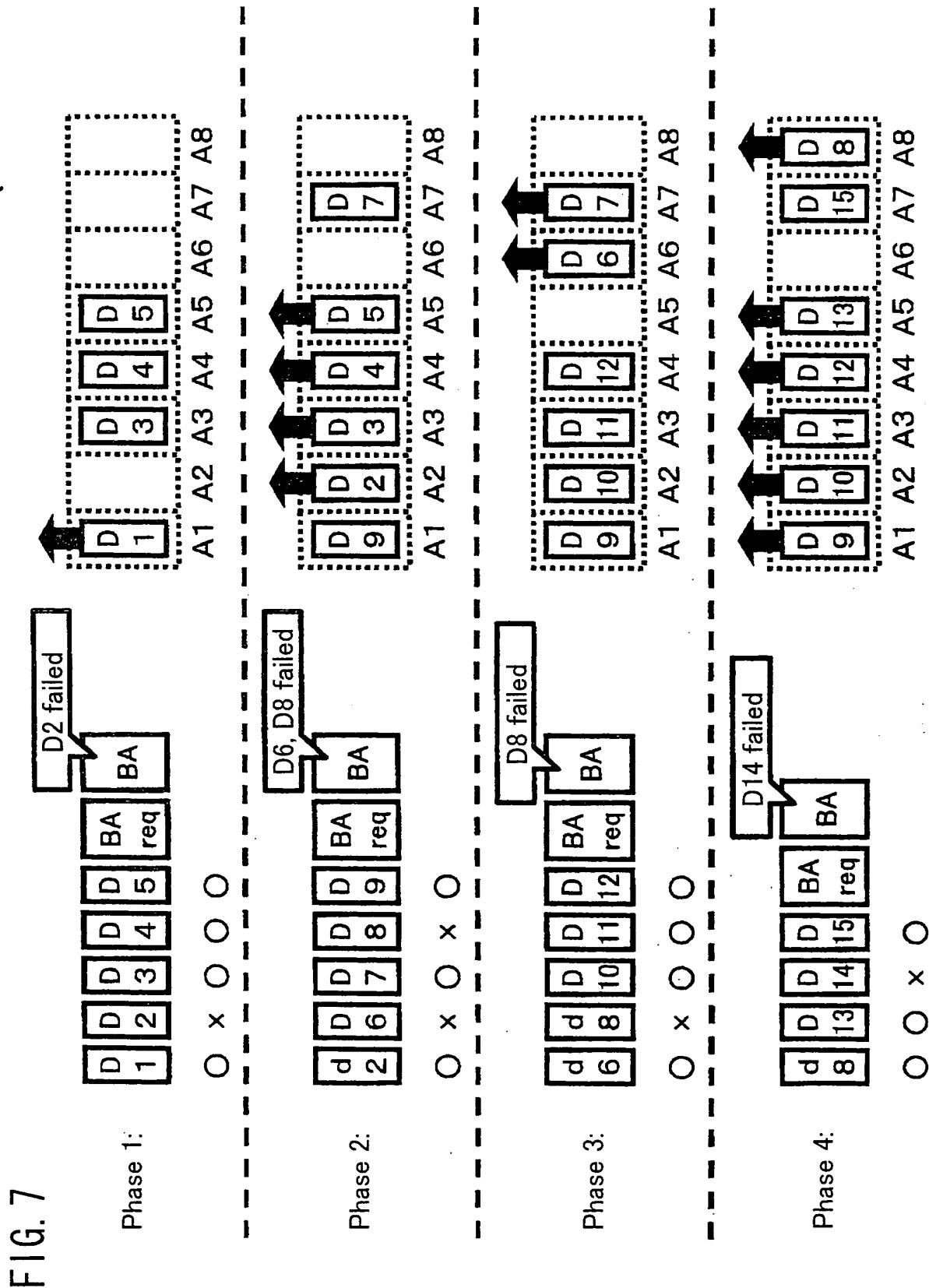
6 / 1 4

FIG. 6

Channel
Buffer in receiving station

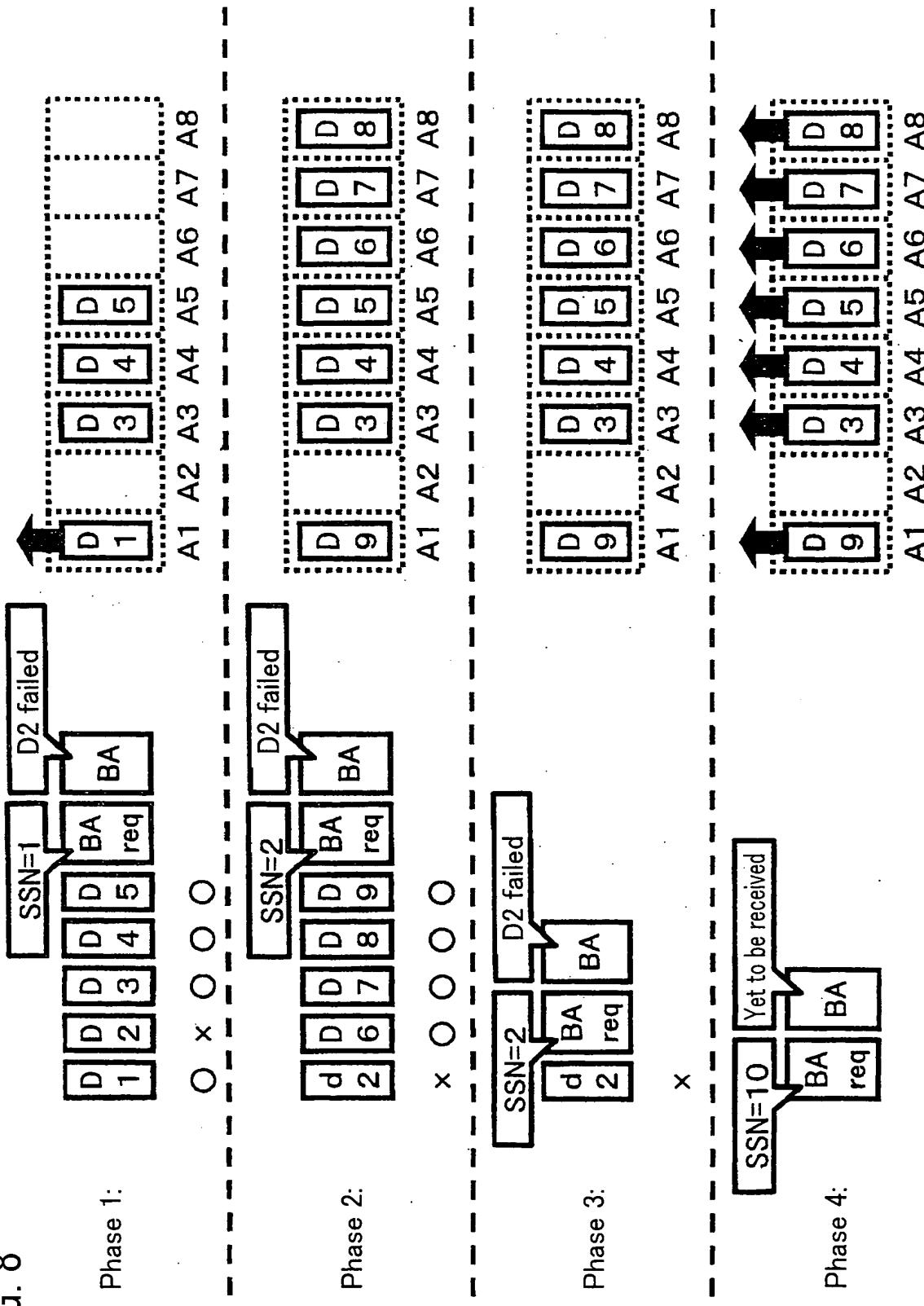


7 / 1 4

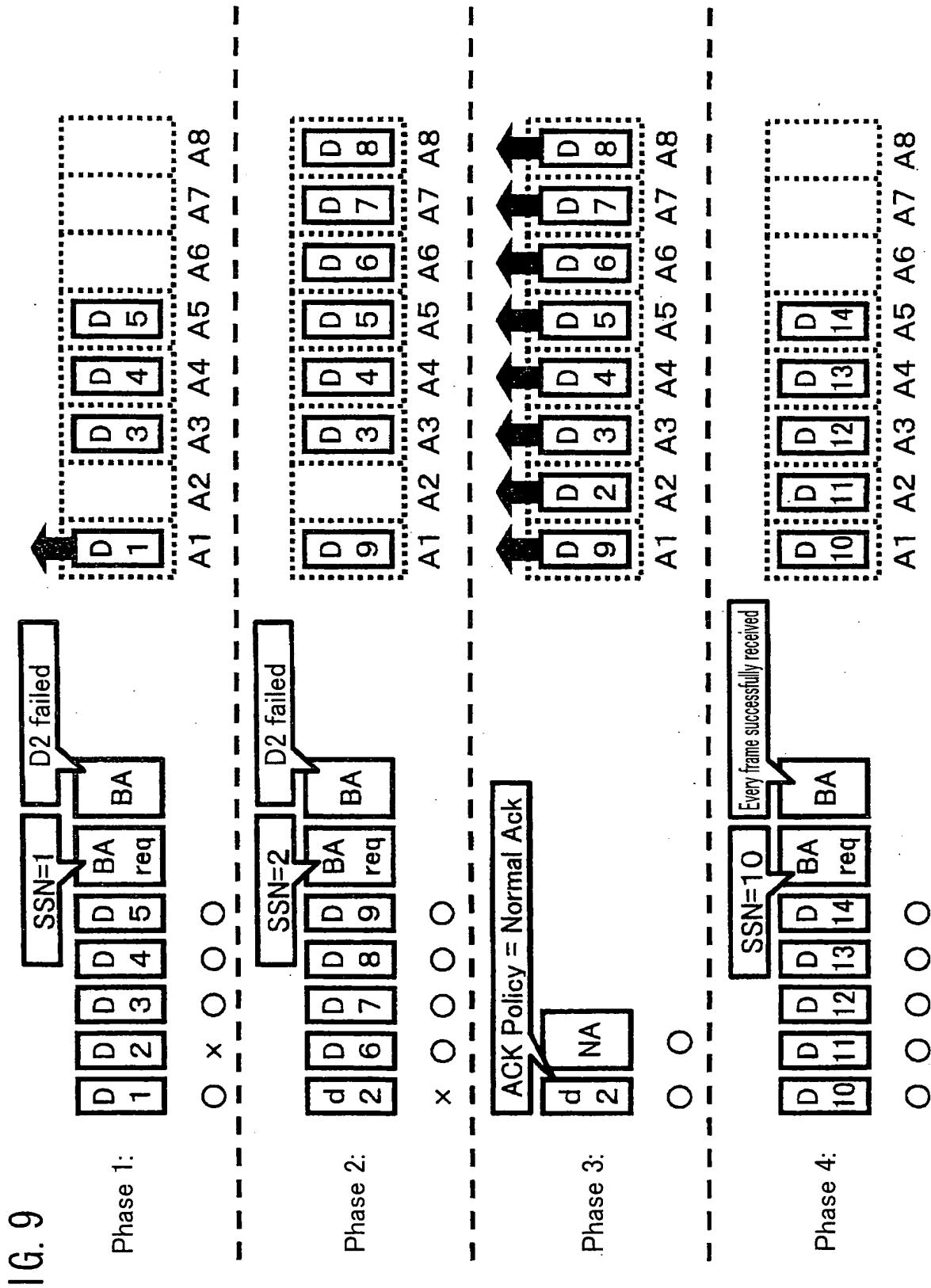


8 / 1 4

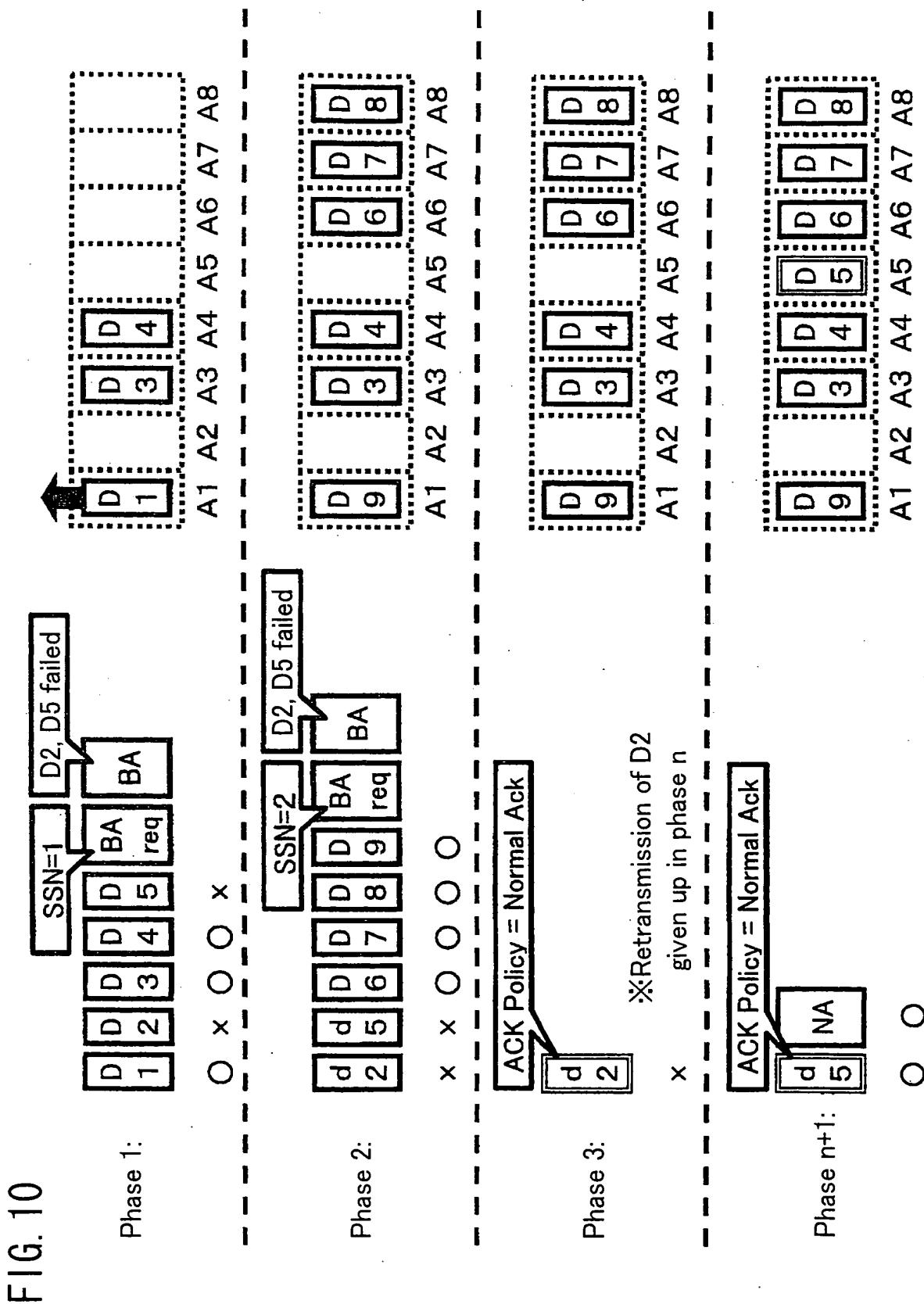
FIG. 8



9 / 1 4

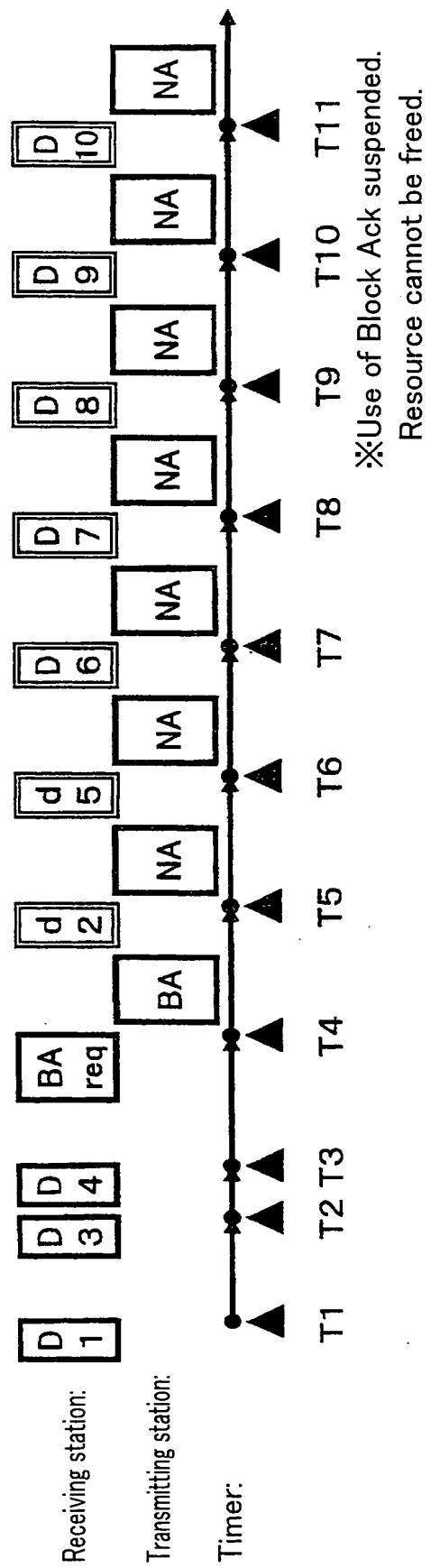


10 / 14



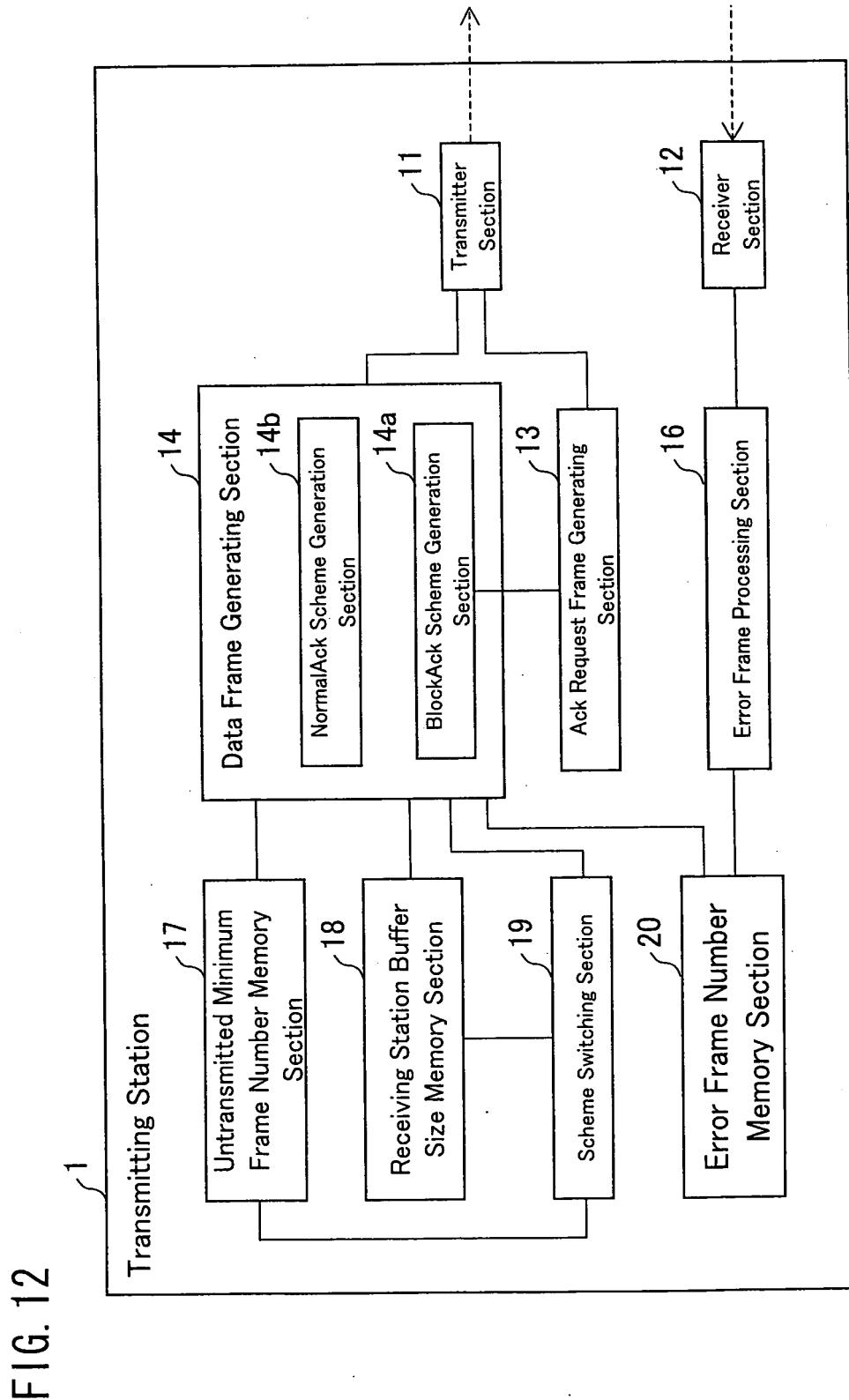
1 1 / 1 4

FIG. 11



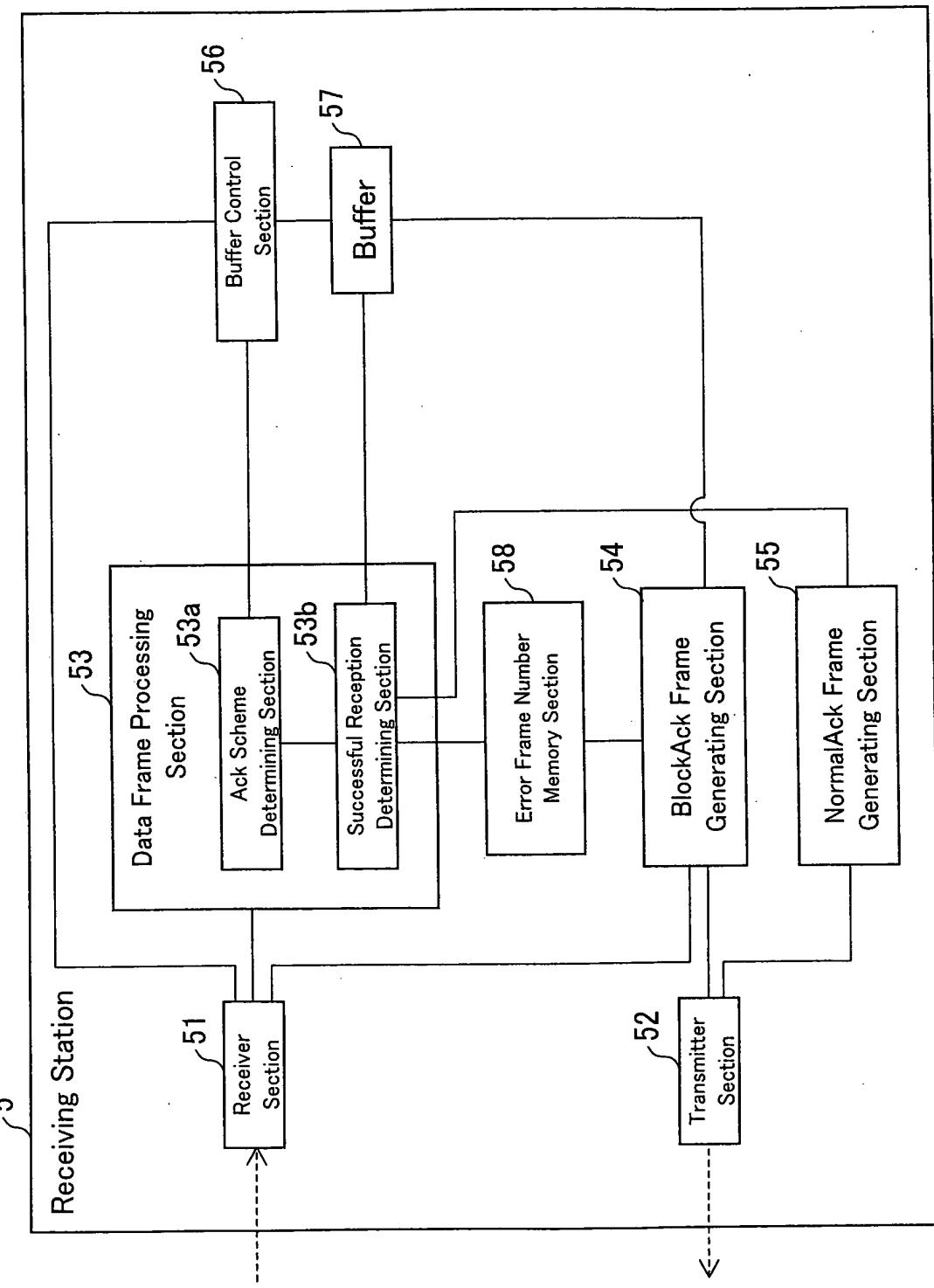
▲ : Timer reset

1 2 / 1 4



13 / 14

FIG. 13



14 / 14

FIG. 14
105

